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Substitute For PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-612001	Application No. 10/039,289
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant Gilbert Wolrich et al.	RECEIVED
(37 CFR §1.98(b))		Filing Date 01/04/02	Group Art Unit 2177 JUL 0 2 2004

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U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	09/475,614	12/1999	Wolrich, et al.			
	AB	09/473,571	12/1999	Wolrich, et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	No
	AC	WO 01/50679	07/2001	WIPO				
	AD	WO 01/50247	07/2001	WIPO				
	AE	WO 01/48619	07/2001	WIPO				
	AF	WO 01/48606	07/2001	WIPO				
	AG	WO 01/48596	07/2001	WIPO				
	AH	WO 01/16782	03/2001	WIPO				
	AI	WO 01/16770	03/2001	WIPO				
	AJ	WO 01/16769	03/2001	WIPO				
	AK	WO 01/15718	03/2001	WIPO				
	AL	WO 97/38372	10/1997	WIPO				
	AM	WO 94/15287	07/1994	WIPO				
	AN	EP 0 809 180	11/1997	Europe				
	AO	EP 0 745 933	12/1996	Europe				
	AP	EP 0 633 678	01/1995	Europe				
	AQ	EP 0 464 715	01/1992	Europe				
	AR	EP 0 379 709	08/1990	Europe				
	AS	59-111533	06/1984	Japan (w/abstract)				X

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AT	Byrd et al., "Multithread Processor Architectures," *IEEE Spectrum*, Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
	AU	Doyle et al., *Microsoft Press Computer Dictionary*, 2nd ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.

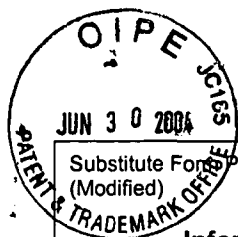| Examiner Signature /Khanh Pham/	Date Considered 05/16/2008

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KP/

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	AV	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
	AW	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," *Journal of Parallel and Distributed Computing*, Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
	AX	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
	AY	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.
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	ACC	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
	ADD	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
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	AFF	Turner et al., "Design of a High Performance Active Router," Internet Document, *Online*, pp. 1-20, 18 March 1999.
	AGG	Vibhatavanij et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-369.
	AHH	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.

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